UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Andrew TOMERLIN	Group/Art Unit:	2816
Application No.:	10/767,088	Examiner:	Ann T. LUU
Filed:	January 29, 2004	Confirmation No.	4603
Title:	CONFIGURABLE DELAY LINE CIRCUIT		

AMENDMENT

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This communication is responsive to the Advisory Action mailed March 27, 2006, concerning the above-identified application. Applicant submits the following Amendment and Remarks and respectfully requests the Examiner to reconsider the application and allow the claims, as amended, to issue. A Petition for Extension of Time to respond, with fee authorization, is submitted concurrently herewith.

Please amend the application as follows:

Amendments to the Specification begin on page 2 of this paper.
Amendments to the Claims are reflected in the listing of claims, which begins on page 3 of is paper.
Remarks/Arguments begin on page 8 of this paper.

Amendments to the Specification:

Please amend the specification by inserting as the first paragraph of the specification: --"Cross Reference to Related Applications". This is a continuation of Application Serial No. 10/767,088 filed January 29, 2004, and assigned to Motorola, Inc.--.

Amendment to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (currently amended) A configurable circuit, comprising:

a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs;

the variable length delay line having a number of active delay elements determined by a program command; and

a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements, the configurable processing array generating a periodic output in response to each program command.

2. (Original) The configurable circuit according to claim 1, further comprising a control processor that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements.

3. (Currently Amended) The configurable circuit according to claim 1, wherein the delay of the N delay elements is controlled by a control processor, the control processor comprising one of: data information logic in conjunction with an arithmetic logic unit (ALU), data formatting logic in conjunction with a multiplexer, and multiplexer in conjunction with an ALU.

4. (Original) The configurable circuit according to claim 1, wherein the delay of the N delay elements is controlled by an output of a delay locked loop.

5. (Original) The configurable circuit according to claim 1, wherein each of the N delay elements comprises a pair of series connected inverters.

6. (Original) The configurable circuit according to claim 1, wherein the configurable processing array further comprises an input and an output that can be configured under program control.

7. (Original) The configurable circuit according to claim 1, wherein the configurable processing array further comprises a plurality of outputs that can be configured under program control.

8. (previously presented) The configurable circuit according to claim 1, wherein the configurable processing array comprise a plurality of configurable processing units (PUs).

9. (previously presented) The configurable circuit according to claim 1, wherein the configurable processing array comprise a programmable logic device.

10. (previously presented) The configurable circuit according to claim 1, further comprising a programmable multiplexer, responsive to a program control command to selectively enable a selected group of delay elements while disabling remaining delay elements.

11. (currently amended) A configurable circuit, comprising:

a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs;

the N delay elements each comprising a pair of series connected inverters;

the variable length delay line having a number of active delay elements determined by a program command;

a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements, the configurable processing array generating a periodic output in response to the program command;

a control processor that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements; and

a delay locked loop controlling the delay of the N delay elements.

12. (currently amended) The configurable circuit according to claim 11, wherein the configurable processing array further comprises an input, and wherein the configurable processor array input and ~~an~~ output ~~that can be~~ are configured under program control of a control processor including one of: data formatting logic in conjunction with an arithmetic logic unit (ALU), data formatting logic in conjunction with a multiplexer, and multiplexer in conjunction with an ALU.

13. (Original) The configurable circuit according to claim 11, wherein the configurable processing array further comprises a plurality of outputs that can be configured under program control.

14. (Original) The configurable circuit according to claim 11, wherein the configurable circuits comprise a plurality of configurable processing units (PUs).

15. (Original) The configurable circuit according to claim 11, wherein the configurable circuits comprise a programmable logic device.

16. (Original) The configurable circuit according to claim 11, further comprising a programmable multiplexer, responsive to the program control command to selectively enable a selected group of delay elements while disabling remaining delay elements.

17. (currently amended) A method of performing a circuit function, comprising:

applying an input to a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs, the variable length delay line having a number of active delay elements determined by a program command; and

applying the delayed outputs of the active delay elements to a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements that have been configured under program control to carry out a circuit function wherein a periodic output is generated in response to the program control.

18. (Original) The method according to claim 17, further comprising programming the variable length delay line and the configurable processing array using a control processor that configures the number of active delay elements of the variable length delay line and configures the circuit function of the array of configurable circuit elements.

19. (Original) The method according to claim 17, further comprising controlling the delay of the N delay elements to achieve a selected overall delay.

20. (currently amended) The method according to claim 17, wherein the configurable processing array further comprises an input and an output that are configured under program control, the configurable processing array comprising one of: data formatting logic in conjunction with an arithmetic logic unit (ALU), data formatting logic in conjunction with a multiplexer, and a multiplexer in conjunction with an ALU.

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21. (Original) The method according to claim 17, wherein the configurable circuits comprise at least one of a plurality of configurable processing units (PUs) and a programmable logic device.

Claims 22 – 28 (Canceled)

29. (currently amended) A configurable circuit, comprising:

a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs, wherein each of the N delay elements comprises a pair of series connected inverters;

the variable length delay line having a number of active delay elements determined by a program command;

a configurable processing array comprising a plurality of configurable processing units (PUs), the configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements;

wherein the configurable processing array further comprises an input and a plurality of outputs that can be configured under program control; and

a control processor that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements and wherein the delay of the N delay elements is controlled by a control processor, wherein the configurable processing array generates a periodic output in response each program command.

REMARKS/ARGUMENT

The claims have been amended by rewriting claims 1, 3, 11, 12, 17, 20 and 29 without prejudice or disclaimer. Reconsideration is respectfully requested.

Regarding the Rejections under 35 U.S.C. §102
Claims 1-4, 6-10 and 17-21 were rejected as anticipated by the Yokota reference of record.
Regarding the Rejections under 35 U.S.C. §103
Claims 5, 11-16 and 29 were rejected as anticipated by the Yokota (US 5,712,582) in view of Lee (US 5,901,190).

Applicants respectfully traverse in part and amend in part. As to independent claims 1, 11, 17 and 29, the input 24 into Applicant's delay line 10 does not change based on the reconfiguration. Yokota's input to delay line (120), on the other hand, does change in response to the reconfiguration because of the feedback path, as seen in FIG. 1. Applicants' input 24 to delay line 10 and data out 42 are not tied together (no feedback) and are thus structurally distinguishable from the Yokota reference.

Applicants have also amended the independent claims to recite that the configurable processing array generates a periodic output in response to each program command. No new matter has been added. Support for this amendment is found on page, 9, lines 9-17. None of the cited references taken individually or combined teach this claimed aspect of the invention. Dependent claims 3, 12 and 20 have also been amended to include that the control processor comprises one of: data information logic in conjunction with an arithmetic logic unit (ALU), data formatting logic in conjunction with a multiplexer, and multiplexer in conjunction with an ALU. Support for this amendment is found in FIGs. 3, 4 and 5 along with the accompanying text found on page 7, lines 29-30 through page 9, line 17. Neither Yokota nor Lee taken individually or combined teach this claimed aspect of the invention. The Examiner equates element (160) of Yokota to a control processor. However, Yokota's element (160) is a decoder. The claims, as amended, further distinguish Applicants' control processor and are thus believed to be in condition for allowance. Neither reference taken individually or

combined teaches that which is claimed by Applicants' invention. The remaining claims are dependent claims providing further limitations to what are believed to be allowable claims and hence are also in condition for allowance.

Accordingly, claims 1-4, 6-10 and 17-21 and claims 5, 11-16 and 29 are believed to be in condition for allowance. Reconsideration is respectfully requested.

The undersigned additionally notes that many other distinctions exist between the cited art and the claims. However, in view of the clear distinctions pointed out above, further discussion is believed to be unnecessary at this time. Failure to address each point raised in the Office Action should accordingly not be viewed as accession to the Examiner's position or an admission of any sort.

No amendment made herein was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim unless an argument has been made herein that such amendment has been made to distinguish over a particular reference or combination of references.

In view of this communication, all claims are now believed to be in condition for allowance and such is respectfully requested at an early date. If further matters remain to be resolved, the undersigned respectfully requests the courtesy of an interview. The undersigned can be reached at the telephone number below.

The Commissioner is hereby authorized to charge Deposit Account 502117, Motorola, Inc, with any fees which may be required in the prosecution of this application.

May 9, 2006 Respectfully submitted,